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## Code No.: 14452 O

## VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD

Accredited by NAAC with A++ Grade

## B.E. (E.C.E.) IV-Semester Backlog Examinations, August-2022 Digital System Design

Time: 3 hours

Max. Marks: 60

Note: Answer all questions from Part-A and any FIVE from Part-B

<ul> <li>Q. No.   Stem of the question</li> <li>1.   Convert Decimal Number (67.66) to its equivalent (i) Binary (ii) Hexa Decimal Numbers.</li> <li>2.   Using Boolean Algebra simplify A+AB + ABC.</li> <li>3.   Identify the advantages and disadvantages of Carry Look Ahead Adder over Ripple Carry Adder.</li> <li>4.   Draw the Logic circuit of 4X2 Priority Encoder.</li> <li>5.   Define Race Around Condition in Flip Flops and Mention the method to eliminate this condition.</li> <li>6.   The content of a 5-bit shift register serial in parallel out with rotation capability is initially 11001. The register is shifted four times to the right. What are the content and the output of the register after each shift?</li> <li>7.   What is the difference between \$stop and \$finish.</li> <li>8.   Define the delays associated with GATE level Modeling.</li> <li>9.   Write the syntax of Tasks and Functions.</li> <li>10.   Design 4X1 mux using conditional operator.</li> <li>11.   a)   State and Prove De Morgan's Theorem.</li> <li>12.   a)   Minimize the following Boolean function using Karnaugh Map.</li> <li>F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)</li> <li>12.   a)   Implement F(A, B, C, D) = ∑ m(0, 1, 5, 6, 8, 10, 12, 15) using 8: 1 multiplexer.</li> <li>  b)   A combinational circuit is defined by the following three Boolean functions. (Use only NAND gates).</li> <li>13.   a)   Draw the state diagram and state table of a Moore FSM to detect the sequence 10110.</li> <li>  b)   Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.</li> <li>14.   a)   Explain the following data types used in Verilog with examples. (i) nets (ii) time (iii) parameters (iv) real</li> <li>  b)   Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.</li> <li>  15.   a)   Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples. (i) nets (ii) time</li></ul>		$Part-A (10 \times 2 = 20 Marks)$				
2. Using Boolean Algebra simplify A+AB+ABC. 3. Identify the advantages and disadvantages of Carry Look Ahead Adder over Ripple Carry Adder. 4. Draw the Logic circuit of 4X2 Priority Encoder. 5. Define Race Around Condition in Flip Flops and Mention the method to eliminate this condition. 6. The content of a 5-bit shift register serial in parallel out with rotation capability is initially 11001. The register is shifted four times to the right. What are the content and the output of the register after each shift? 7. What is the difference between \$stop and \$finish. 2 1 4 2  8. Define the delays associated with GATE level Modeling. 9. Write the syntax of Tasks and Functions. 10. Design 4X1 mux using conditional operator. 11. a) State and Prove De Morgan's Theorem. b) Minimize the following Boolean function using Karnaugh Map. F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)  11. a) Minimize the following Boolean function using Karnaugh Map. F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)  12. a) Implement F(A, B, C, D) = Σm(0, 1, 5, 6, 8, 10, 12, 15) using 8: 1 multiplexer. b) A combinational circuit is defined by the following three Boolean functions: (Use only NAND gates).  13. a) Draw the state diagram and state table of a Moore FSM to detect the sequence 10110. b) Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.  14. a) Explain the following data types used in Verilog with examples. b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality. 15. a) Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples. b) Write the Verilog Code for 4 bit Up Counter using if-else statements. c) Draw the Circuit of BCD adder and explain its working. c) Answer any noo of the following: a) Draw the Switch	Q. No.	Stem of the question	M	L	CO	PO
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<ul> <li>Part-B (5 x 8 = 40 Marks)</li> <li>State and Prove De Morgan's Theorem.</li> <li>Minimize the following Boolean function using Karnaugh Map.</li> <li>F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)</li> <li>Implement F(A, B, C, D) = ∑ m(0, 1, 5, 6, 8, 10, 12, 15) using 8: 1 multiplexer.</li> <li>A combinational circuit is defined by the following three Boolean functions: (Use only NAND gates).</li> <li>Draw the state diagram and state table of a Moore FSM to detect the sequence 10110.</li> <li>Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.</li> <li>Explain the following data types used in Verilog with examples.</li> <li>(i) nets (ii) time (iii) parameters (iv) real</li> <li>Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.</li> <li>Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.</li> <li>Write the Verilog Code for 4 bit Up Counter using if-else statements.</li> <li>Classify the Binary Codes. Give one example to each one.</li> <li>Draw the Circuit of BCD adder and explain its working.</li> <li>Answer any two of the following:</li> <li>With a neat diagram explain 4 bit Ring Counter.</li> <li>Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.</li> <li>4 2 4 2</li> </ul>	9.	Write the syntax of Tasks and Functions.	2	1	5	2
11. a) State and Prove De Morgan's Theorem. b) Minimize the following Boolean function using Karnaugh Map. F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)  12. a) Implement F(A, B, C, D) = ∑ m(0, 1, 5, 6, 8, 10, 12, 15) using 8:1 multiplexer. b) A combinational circuit is defined by the following three Boolean functions: F1=X'Y'Z'+XZ and F2=X'YZ'+X'Y. Design the circuit that implements the functions. (Use only NAND gates).  13. a) Draw the state diagram and state table of a Moore FSM to detect the sequence 10110. b) Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.  14. a) Explain the following data types used in Verilog with examples. (i) nets (ii) time (iii) parameters (iv) real b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  15. a) Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples. b) Write the Verilog Code for 4 bit Up Counter using if-else statements. c) Draw the Circuit of BCD adder and explain its working. 4 2 4 2 2 2 2 3 2 3 2 3 2 3 3 3 3 3 3 3	10.	Design 4X1 mux using conditional operator.	2	3	5	3
b) Minimize the following Boolean function using Karnaugh Map.  F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)  Implement F(A, B, C, D) = ∑ m(0, 1, 5, 6, 8, 10, 12, 15) using 8:1 multiplexer.  A combinational circuit is defined by the following three Boolean functions: F1=X'Y'Z'+XZ and F2=X'YZ'+X'Y. Design the circuit that implements the functions. (Use only NAND gates).  Draw the state diagram and state table of a Moore FSM to detect the sequence 10110.  b) Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.  14. a) Explain the following data types used in Verilog with examples. (i) nets (ii) time (iii) parameters (iv) real  Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.  b) Write the Verilog Code for 4 bit Up Counter using if-else statements.  4 3 5 3 4 1 2 2 2 2 2 3 2 3 2 3 2 3 2 3 2 3 2 3 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3		Part-B $(5 \times 8 = 40 \text{ Marks})$	1			
F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)  12. a) Implement F(A, B, C, D) = ∑ m(0, 1, 5, 6, 8, 10, 12, 15) using 8 : 1 multiplexer.  A combinational circuit is defined by the following three Boolean functions: F1=X'Y'Z'+XZ and F2=X'YZ'+X'Y. Design the circuit that implements the functions. (Use only NAND gates).  13. a) Draw the state diagram and state table of a Moore FSM to detect the sequence 10110.  b) Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.  14. a) Explain the following data types used in Verilog with examples. (i) nets (ii) time (iii) parameters (iv) real b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  15. a) Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples. b) Write the Verilog Code for 4 bit Up Counter using if-else statements. 4 3 5 3 16. a) Classify the Binary Codes. Give one example to each one. b) Draw the Circuit of BCD adder and explain its working. 4 2 2 2 2 7 8 9 2 4 2 9 3 2 9 3 2 9 3 2 9 3 2 9 3 2 4 2 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 4 2 9 6 8 6 7 8 10 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7	11. a)	State and Prove De Morgan's Theorem.	4	2	1	2
<ul> <li>12. a) Implement F(A, B, C, D) = ∑ m(0, 1, 5, 6, 8, 10, 12, 15) using 8 : 1 multiplexer. A combinational circuit is defined by the following three Boolean functions: F1=X'Y'Z'+XZ and F2=X'YZ'+X'Y. Design the circuit that implements the functions. (Use only NAND gates).</li> <li>13. a) Draw the state diagram and state table of a Moore FSM to detect the sequence 10110. Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops. Explain the following data types used in Verilog with examples. (i) nets (ii) time (iii) parameters (iv) real</li> <li>b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.</li> <li>15. a) Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.</li> <li>b) Write the Verilog Code for 4 bit Up Counter using if-else statements.</li> <li>b) Urite the Verilog Code so Give one example to each one.</li> <li>b) Draw the Circuit of BCD adder and explain its working.</li> <li>d) Answer any two of the following:</li> <li>d) Answer any two of the following:</li> <li>d) Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.</li> <li>d) Urite the Verilog Code.</li> <li>d) Urite the Verilog Code.</li> <li>d) Urite the Switch Level Circuit for 2 input AND gate and Verilog Code.</li> </ul>	b)	Minimize the following Boolean function using Karnaugh Map.	4	3	1	2
b) A combinational circuit is defined by the following three Boolean functions:  F1=X'Y'Z'+XZ and F2=X'YZ'+X'Y. Design the circuit that implements the functions.  (Use only NAND gates).  13. a) Draw the state diagram and state table of a Moore FSM to detect the sequence 10110.  b) Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.  Explain the following data types used in Verilog with examples.  (i) nets (ii) time (iii) parameters (iv) real  b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.  b) Write the Verilog Code for 4 bit Up Counter using if-else statements.  4 3 5 2  Write the Verilog Code So Give one example to each one.  b) Draw the Circuit of BCD adder and explain its working.  Answer any two of the following:  a) With a neat diagram explain 4 bit Ring Counter.  Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.		$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$				
b) A combinational circuit is defined by the following three Boolean functions:  F1=X'Y'Z'+XZ and F2=X'YZ'+X'Y. Design the circuit that implements the functions.  (Use only NAND gates).  13. a) Draw the state diagram and state table of a Moore FSM to detect the sequence 10110.  b) Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.  Explain the following data types used in Verilog with examples.  (i) nets (ii) time (iii) parameters (iv) real  b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.  b) Write the Verilog Code for 4 bit Up Counter using if-else statements.  4 3 5 2  Write the Verilog Code So Give one example to each one.  b) Draw the Circuit of BCD adder and explain its working.  Answer any two of the following:  a) With a neat diagram explain 4 bit Ring Counter.  Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.	12. a)	Implement $F(A, B, C, D) = \sum m(0, 1, 5, 6, 8, 10, 12, 15)$ using 8:1 multiplexer.	4	4	2	2
F1=X'Y'Z'+XZ and F2=X'YZ'+X'Y. Design the circuit that implements the functions. (Use only NAND gates).  13. a) Draw the state diagram and state table of a Moore FSM to detect the sequence 10110. b) Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.  Explain the following data types used in Verilog with examples. (i) nets (ii) time (iii) parameters (iv) real b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples. b) Write the Verilog Code for 4 bit Up Counter using if-else statements.  Classify the Binary Codes. Give one example to each one. b) Draw the Circuit of BCD adder and explain its working.  Answer any two of the following:  With a neat diagram explain 4 bit Ring Counter. b) Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.	b)	A combinational circuit is defined by the following three Boolean functions:	4	2	2	2
13. a) Draw the state diagram and state table of a Moore FSM to detect the sequence 10110.  b) Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.  14. a) Explain the following data types used in Verilog with examples.  (i) nets (ii) time (iii) parameters (iv) real  b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  15. a) Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.  b) Write the Verilog Code for 4 bit Up Counter using if-else statements.  c) Draw the Circuit of BCD adder and explain its working.  17. Answer any two of the following:  with a neat diagram explain 4 bit Ring Counter.  b) Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.  4 2 4 2  4 2 4 2  5 3 2  4 2 4 2  4 2 4 2  4 3 5 3  5 2  6 3 3  6 4 3 4 1  7 5 2  8 7 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7						
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4, 5, 6, 7. Use JK flip-flops.  Explain the following data types used in Verilog with examples.  (i) nets (ii) time (iii) parameters (iv) real  b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  15. a) Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.  b) Write the Verilog Code for 4 bit Up Counter using if-else statements.  4 3 5 2  Write the Verilog Code for 4 bit Up Counter using if-else statements.  4 3 5 3  16. a) Classify the Binary Codes. Give one example to each one.  b) Draw the Circuit of BCD adder and explain its working.  4 2 2 2  17. Answer any two of the following:  with a neat diagram explain 4 bit Ring Counter.  b) Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.  4 2 4 2	13. a)	Draw the state diagram and state table of a Moore FSM to detect the sequence 10110.	4	3	3	2
Explain the following data types used in Verilog with examples.  (i) nets (ii) time (iii) parameters (iv) real  b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  15. a) Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.  b) Write the Verilog Code for 4 bit Up Counter using if-else statements.  4 3 5 2 with examples.  b) Write the Verilog Code for 4 bit Up Counter using if-else statements.  4 3 5 3 4 1 4 3 5 2 4 5 2 4 2 5 1 2 5 1 2 5 1 2 5 1 2 1 2 5 1 2 1 2	b)		4	4	3	3
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b) Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.  15. a) Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.  b) Write the Verilog Code for 4 bit Up Counter using if-else statements. 4 3 5 2  Write the Verilog Code for 4 bit Up Counter using if-else statements. 4 3 5 3  16. a) Classify the Binary Codes. Give one example to each one. 4 2 1 2  b) Draw the Circuit of BCD adder and explain its working. 4 2 2 2  17. Answer any two of the following: 4 2 3 2  With a neat diagram explain 4 bit Ring Counter.  b) Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.  4 2 4 2		The state of the s		2	7	
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17. Answer any <i>two</i> of the following:  a) With a neat diagram explain 4 bit Ring Counter.  b) Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.  4 2 4 2	b)					
a) With a neat diagram explain 4 bit Ring Counter. b) Draw the Switch Level Circuit for 2 input AND gate and Verilog Code. 4 2 4 2	17.		4			
	a)	With a neat diagram explain 4 bit Ring Counter.				
	b)		4	2	4	2
	c)		4	2	5	2

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level - 3 & 4	40%