Hall Ticket Number:

Code No. : 14452 O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) IV-Semester Backlog Examinations, August-2022

Digital System Design

Time: 3 hours Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10× 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Convert Decimal Number (67.66) to its equivalent (i) Binary (ii) Hexa Decimal Numbers.	2	1	1	1
2.	Using Boolean Algebra simplify A+AB + ABC.	2	1	1	1
3.	Identify the advantages and disadvantages of Carry Look Ahead Adder over Ripple Carry Adder.	2	1	2	2
4.	Draw the Logic circuit of 4X2 Priority Encoder.	2	1	2	1
5.	Define Race Around Condition in Flip Flops and Mention the method to eliminate this condition.	2	1	3	2
6.	The content of a 5-bit shift register serial in parallel out with rotation capability is initially 11001. The register is shifted four times to the right. What are the content and the output of the register after each shift?	2	3	3	3
7.	What is the difference between $stop and $finish.	2	1	4	2
8.	Define the delays associated with GATE level Modeling.	2	1	4	2
9.	Write the syntax of Tasks and Functions.	2	1	5	2
10.	Design 4X1 mux using conditional operator.	2	3	5	3
	Part-B (5 × 8 = 40 Marks)				
11. a)	State and Prove De Morgan's Theorem.	4	2	1	2
b)	Minimize the following Boolean function using Karnaugh Map. $F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$	4	3	1	2
12. a)	Implement $F(A, B, C, D) = \sum m(0, 1, 5, 6, 8, 10, 12, 15)$ using 8 : 1 multiplexer.	4	4	2	2
b)	A combinational circuit is defined by the following three Boolean functions: F1=X`Y`Z`+XZ and F2=X`YZ`+X`Y. Design the circuit that implements the functions. (Use only NAND gates).	4	2	2	2
13. a)	Draw the state diagram and state table of a Moore FSM to detect the sequence 10110.	4	3	3	2
b)	Design a Synchronous Counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use JK flip-flops.	4	4	3	3
14. a)	Explain the following data types used in Verilog with examples. (i) nets (ii) time (iii) parameters (iv) real	4	2	4	2
b)	Write a Verilog HDL code to design 4X1-Multiplexer using Data Flow model and also write the test bench to verify the functionality.	4	3	4	1
15. a)	Distinguish between Blocking and non Blocking assignments supported by Verilog HDL with examples.	4	3	5	2
b)	Write the Verilog Code for 4 bit Up Counter using if-else statements.	4	3	5	3
16. a)	Classify the Binary Codes. Give one example to each one.	4	2	1	2
b)	Draw the Circuit of BCD adder and explain its working.	4	2	2	2
17.	Answer any ***two*** of the following:	4	2	3	2
a)	With a neat diagram explain 4 bit Ring Counter.				
b)	Draw the Switch Level Circuit for 2 input AND gate and Verilog Code.	4	2	4	2
c)	Draw the Logic Synthesis Flow chart and Explain its importance.	4	2	5	2

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%